AMENDMENTS

In the Claims:

This listing of claims replaces all prior versions, and listings, of claims in this application:

1. (Currently Amended) An active matrix display device comprising:

a plurality of pixel element electrodes disposed in a matrix configuration; and

a plurality of retaining circuits ~~disposed~~ provided for the pixel element electrodes[[;]],

wherein the active matrix display device operates under two operation modes, one of said operation modes being a normal operation mode in which the pixel element electrode receives a pixel element voltage in response to an inputted image signal for presenting an analog image, another of said operation modes being a memory operation mode in which a digital image is presented based on a voltage held by the retaining circuit[[;]], and

wherein at least one of the retaining circuits is ~~disposed~~ provided as a common retaining circuit for two or more of the pixel ~~elements~~ element electrodes ~~, and~~ so that an output of the common retaining circuit is shared by said two or more of the pixel element electrodes, and each of said two or more of the pixel element electrodes is connected to only one signal line.

2. (Currently Amended) The active matrix display device of claim 1, wherein [[a]] the common retaining circuit is ~~disposed~~ provided for every two pixel ~~elements~~ element electrodes and the output of the common retaining circuit is shared by said every two pixel element electrodes.

3. (Currently Amended) The active matrix display device of claim 1, wherein [[a]] the common retaining circuit is ~~disposed~~ provided for every four pixel ~~elements~~ element electrodes and the output of the common retaining circuit is shared by said every four pixel element electrodes.

4. (Currently Amended) An active matrix display device comprising:

a plurality of pixel element electrodes disposed in a matrix configuration; and

a plurality of retaining circuits ~~disposed~~ provided for the pixel element electrodes[[;]],

wherein the active matrix display device operates under two operation modes, one of said operation modes being a normal operation mode in which the pixel element electrode receives a pixel element voltage in response to an inputted image signal for presenting an analog image, another of said operation modes being a memory operation mode in which a digital image is presented based on a voltage held by the retaining circuit[[;]], and

wherein ~~the number of the retaining circuits is smaller than the number of the pixel element electrodes~~ at least one of the retaining circuits is provided as a common retaining circuit for two or more of the pixel element electrodes so that an output of the common retaining circuit is applied to all of said two or more of the pixel element electrodes at the same time.

5. (Original) The active matrix display device of claim 4, wherein the number of the retaining circuits is a half of the number of the pixel element electrodes.

6. (Currently Amended) The active matrix display device of claim 4, wherein the number of the retaining circuits is [[1/4]] one fourth of the number of the pixel element electrodes.

7. (Cancelled)

8. (Currently Amended) The active matrix display device of claim [[7]] 4, wherein the number of [[the]] pixel elements for display under the memory operation mode is a half of the number of [[the]] pixel ~~element~~ elements for display under the normal operation mode.

9. (Currently Amended) The active matrix display device of claim [[7]] 4, wherein the number of [[the]] pixel elements for display under the memory operation mode is one fourth of the number of [[the]] pixel ~~element~~ elements for display under the normal operation mode.

10. (Currently Amended) The active matrix display device of claim 1, 2, 3, 4, 5, 6, [[7,]] 8 or 9, wherein the retaining circuit is a multiple-bit memory holding voltages of three or more values.